2/

DISCONTINUED

No.SB-6025

SPECIFICATIONS

for

DOT MATRIX LCD MODULE

EG7004S-AR

640 x 200 dots, 1/100 duty

SEPTEMBER 12, 1986

SEIKO EPSON CORPORATION

3/

EG7004S

TABLE OF CONTENTS

4/

1. DESCRIPTION

The EG7004S is a large-capacity graphic module which consists of a high-contrast, wide angle-of-view 1/100 duty multiplexed STN LCD and CMOS LSIs for LCD driving.
The EG7004S can be display a character 80 columns x 25 rows or 640 horizontal dots x 200 vertical dots, full graphic.

1.1 Features

(1) CMOS LSIs specifically designed to drive LCDs

(2) Large-capacity graphics type capable of displaying numerics, alphabetics, special characters, graphs, charts, and patterns

(3) 4 bits parallel chip enable method for data transfer

(4) STN LCD

(5) Positive display

(6) Refrective type

(7) 1/100 duty multiprexing drive

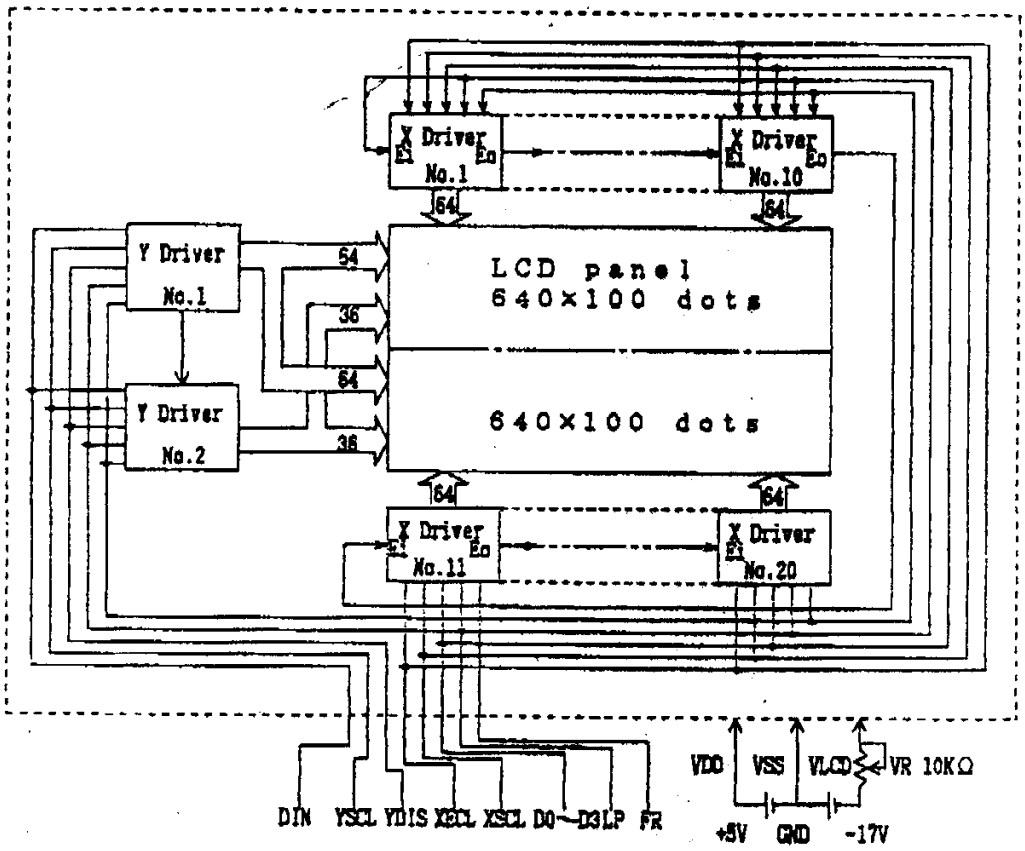
(8) Colors Display dots --- violet

Background ----- gray

2. MECHANICAL SPECIFICATIONS

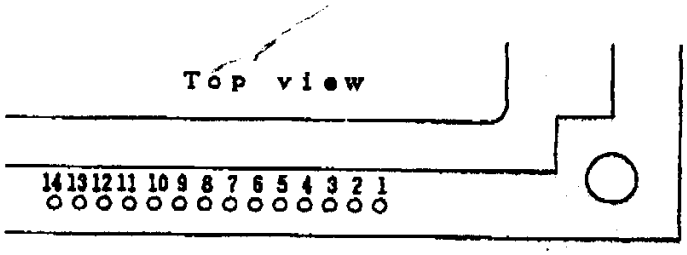
Item	Specifications
Dot matrix	640 x 200 (dots)
Overall dimensions (L x W x D)	290 x 154 x 11.5 (Max) (mm)
Viewing area (L x W)	266 x 119 (mm)
Active area (L x W)	249.56 x 107.96 (mm)
Dot pitch (L x W)	0.39 x 0.54 (mm)
Dot size (L x W)	0.35 x 0.50 (mm)
Weight	Approx 480 (g)

3. BLOCK DIAGRAM



4. I/O TERMINALS

4.1 Terminal Configuration

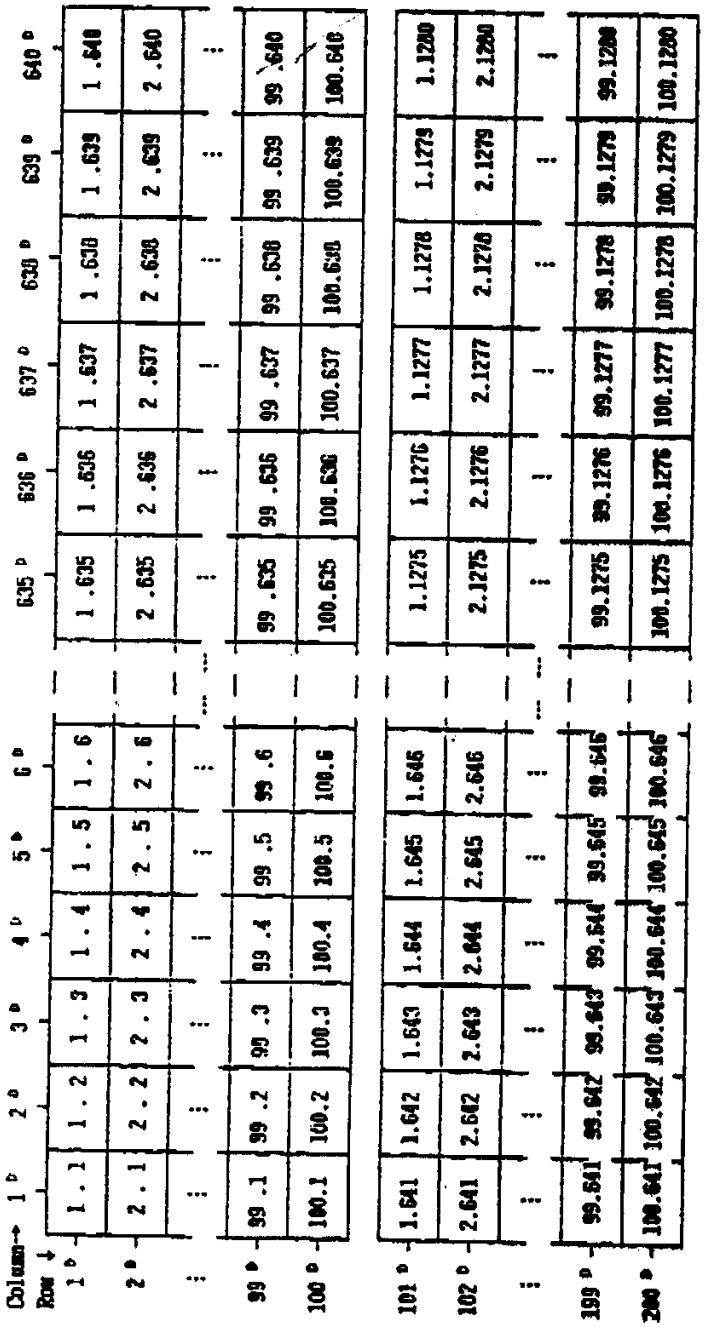


4.2 Terminal Functions

No.	Symbol	Name	Function
1	VDD	Power supply	+5 V ±5%
2	VSS	GND	0 V
3	VLCD	Power supply for LCD panel	VDD-VLCD=22 V MAX
4	LP	Latch pulse	Data latch signal
5	FR	Frame pulse	LCD AC driving signal
6	YDIS	Display control	YDIS="0" Display off YDIS="1" Normal state
7	YSCL	Y shift clock	Row scan shift clock
8	DIN	Synchronizing pulse	Row scan start-up pulse
9	XSCL	X shift clock	Data shift clock
10	XECL	Enable clock	Enable transition clock
11 ~ 14	D0~D3	Data	Display data input

5. DATA INPUT FORMAT
(640 x 100 dots + 640 x 100 dots)

5.1 Display Dot Map



9/

[Note 1] Format "1.2" indicates the first dot (column) the second dot (row).
[Note 2] If data is entered in the block enclosed by dotted lines (201-dot to 208-dot), it will not be displayed.

The previous display dot map shows the entry order of data in terms of dots on the LCD.
Display data is sequentially entered in D0-D3 on a 4 bits basis, from left to right, beginning with location "1.1".
The display consists of two parts: the upper display (640 x 104 dots) and the lower display (640 x 96 dots).
Entry proceeds in the upper display from 1.1 - 1.4, 1.5 - 1.8, ... to 1.640 on a 4 dots (bits) basis.
Then succeeding data enters in the lower display, proceeding from 1.641 to 1.1280. This completes the input of data on the first line (common), followed by entry on the second line, the third line, ...

5.2 Correspondence of Data Input Terminals to Dot Numbers in a Row

Data Input Terminal	Dots (Row) on Display
D0	dot 4, dot 8 ..... dot 1276, dot 1280
D1	dot 3, dot 7 ..... dot 1275, dot 1279
D2	dot 2, dot 6 ..... dot 1274, dot 1278
D3	dot 1, dot 5 ..... dot 1273, dot 1277

Input data D0-D3 correspond to display dots (row) as shown above. The first input data corresponds to dots 4-1, and the last input data to dots 1280-1277.

5.3 Data Input Method

This module uses "Chip Enable Transmission System" to reduce its power consumption. Data is inputted directly into LCD drivers (chips) on a chip basis. If the n-th chip in enable state becomes full of data, the XECL transmits "enable" to the (n+1)th chip allowing subsequent data to be entered in the (n+1)th chip.

"Chip enable" is transmitted at the trailing edge of the XECL. One X-driver (chip) can output a segment equivalent to 64 dots. Therefore, 16 pulses of XSCL are required to input 64 bits of data to each driver.

Supplying a total of 104 lines with data (one line consisting of 1280 dots, equivalent to 20 chips) causes the viewing area of display to become full of data.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Standard Value	Unit
Supply voltage	VDD	0 ~ +7	V
	VSS	GND	
	VLCD	VDD-VLCD≤25 Max	
Input voltage	VIN	VSS≤VIN≤VDD	V
Operating temperature	Top	0 ~ +50	°C
Storage temperature	Tst	-20 ~ +60	

11/

7. ELECTRICAL CHARACTERISTICS

7.1 DC Characteristics

VDD=5V±5%
VSS=0V Top=0~50 oC

Parameter	Symbol	Standard value			Unit	Condition
		Min	Typ	Max		
Supply voltage (Logic)	VDD	4.75	5	5.25	V	VDD
Supply voltage (LCD)	VLCD	VDD-22	-	-	V	VLCD [Note]
"High" input voltage	VIH	0.8VDD	-	VDD	V	
"Low" input voltage	VIL	0	-	0.2VDD	V	
"High" input leakage current	IIH	-	-	50	uA	LP, FR, DIN YDIS, YSCL XSCL, XECL D0~D3
"Low" input leakage current	IIL	-	-	-50	uA	
Input capacitance	CI	-	-	220	pF	
Supply current (Logic)	IDD	-	-	12	mA	VDD :VDD=5V :VLCD=-10V :FR=60Hz
Supply current (LCD)	ILCD	-	-	8	mA	VLCD :VDD=5V :VLCD=-10V :FR=60Hz
Power consumption	PC	-	-	120	mW	:VDD=5V :VLCD=-10V :FR=60Hz

[Note] For the VLCD, see "Vop", section 8 "OPTICAL CHARACTERISTICS".

12/

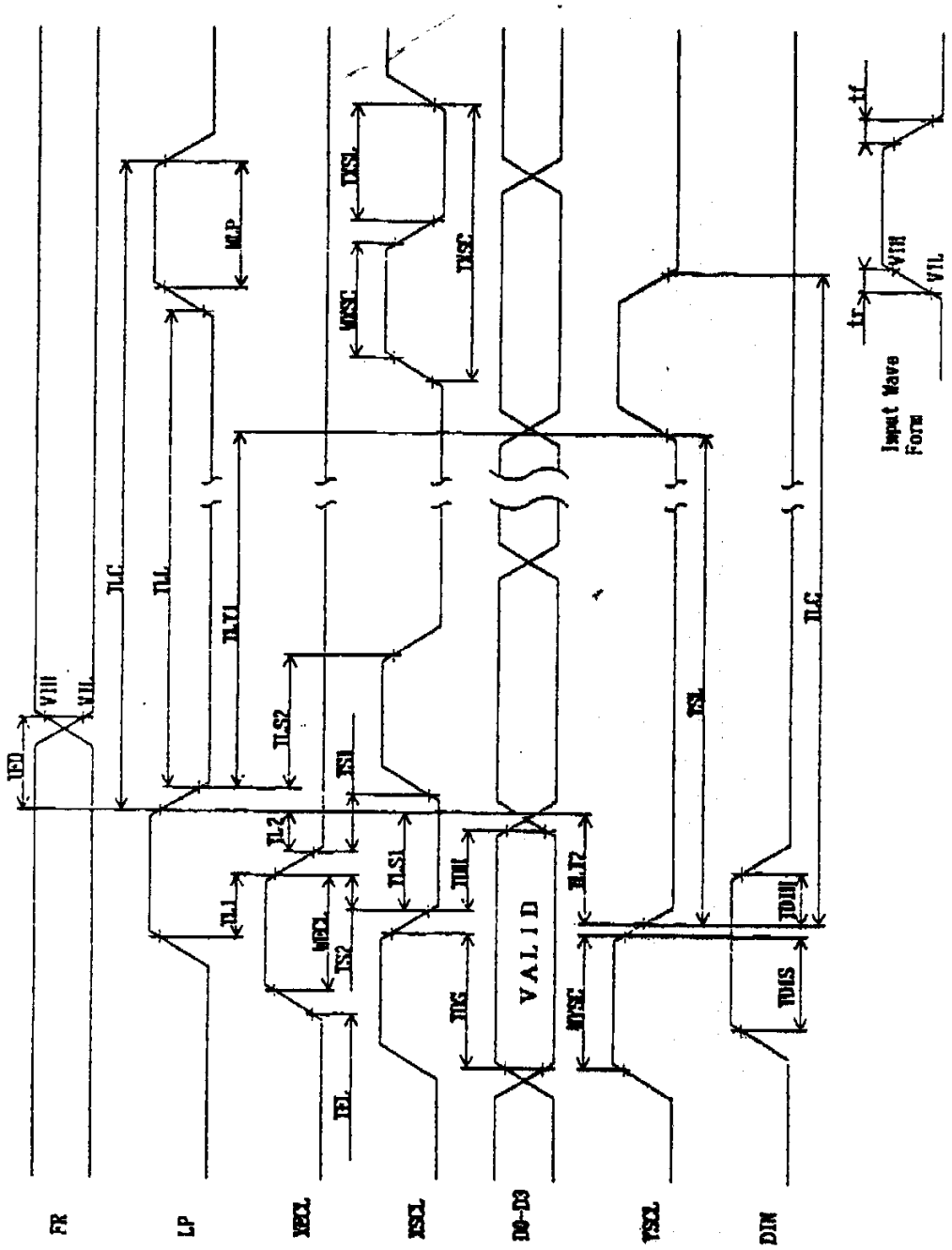
7.2 AC Characteristics

Parameter	Symbol	Standard value			Unit	Condition
		Min	Typ	Max		
FR delay time	TFD	-500	0	500	ns	
LP,YSCL period	TLC	-	140	-	us	
XSCL period	TXSC	166	-	-	ns	
YSCL "L" time	TSL	180	-	-	ns	
YSCL pulse width	WYSC	180	-	-	ns	
LP "L" time	TLL	220	-	-	ns	
LP pulse width	WLP	260	-	-	ns	
XECL "L" time	TEL	100	-	-	ns	
XECL pulse width	WECL	100	-	-	ns	
XSCL "L" time	TXSL	63	-	-	ns	
XSCL pulse width	WXSC	63	-	-	ns	VDD=5V
XECL setup time	TL1	140	-	-	ns	
XECL hold time	TL2	50	-	-	ns	
Latch timing	TLT1 TLT2 TLS1 TLS2	125 0 100 0	- - - -	- - - -	ns	
XECL switching time ("H")	TS1	70	-	-	ns	
XECL switching time ("L")	TS2	-10	-	-	ns	
Data setup time	TDS	50	-	-	ns	
Data hold time	TDH	30	-	-	ns	
DIN setup time	TDIS	100	-	-	ns	
DIN hold time	TDIH	30	-	-	ns	
Rise & Fall time	tr,tf	-	-	*	ns	

* (TXSC-TXSL-WXSC)/2 with 50 ns Max.

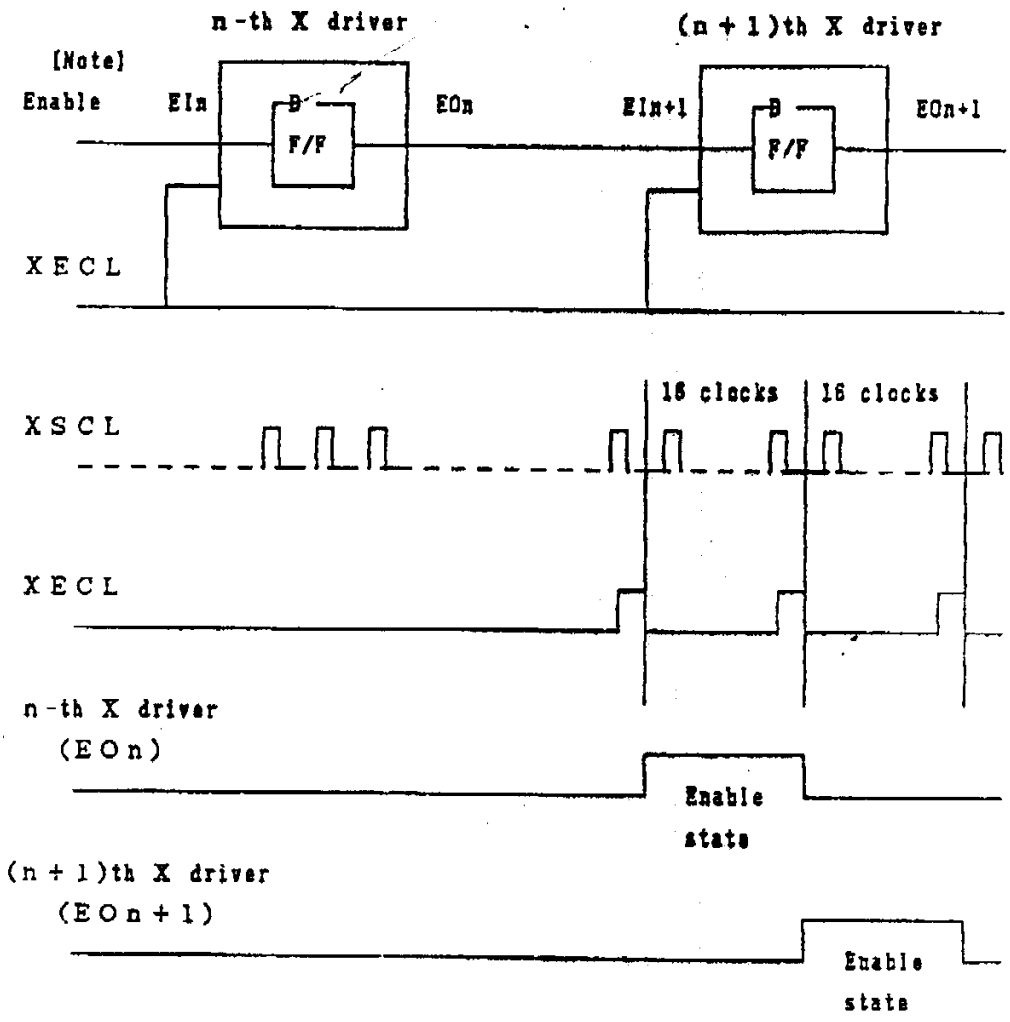
13/

7.2.1 Timing Chart of X(Column) Driver and Y(Row) Driver



14/

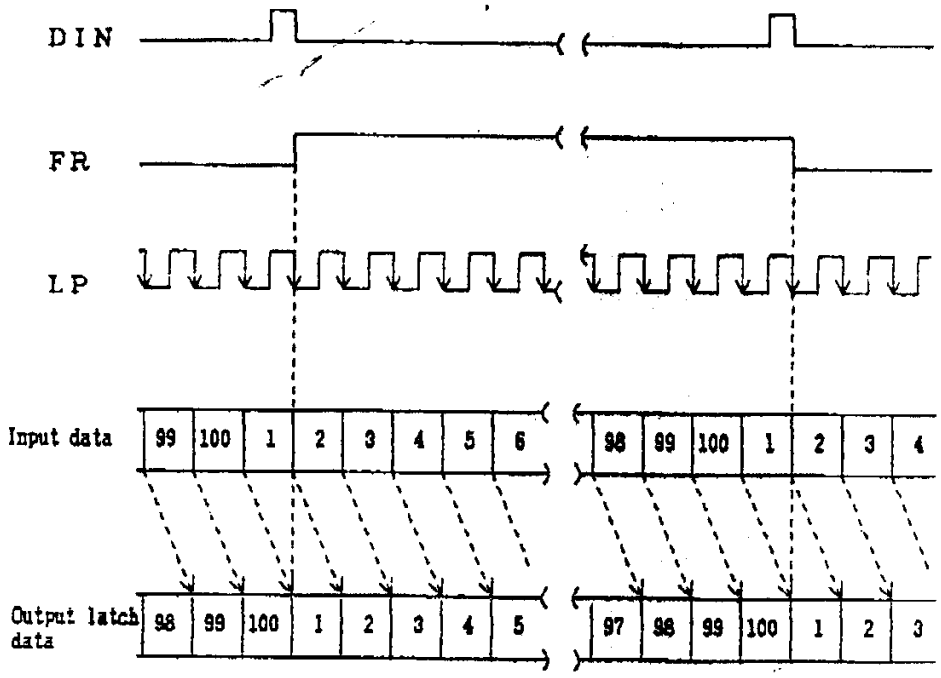
7.2.2 Enable Transition Timing



[Note] Within the module, LP is connected to EI1 of the first chip.

15/

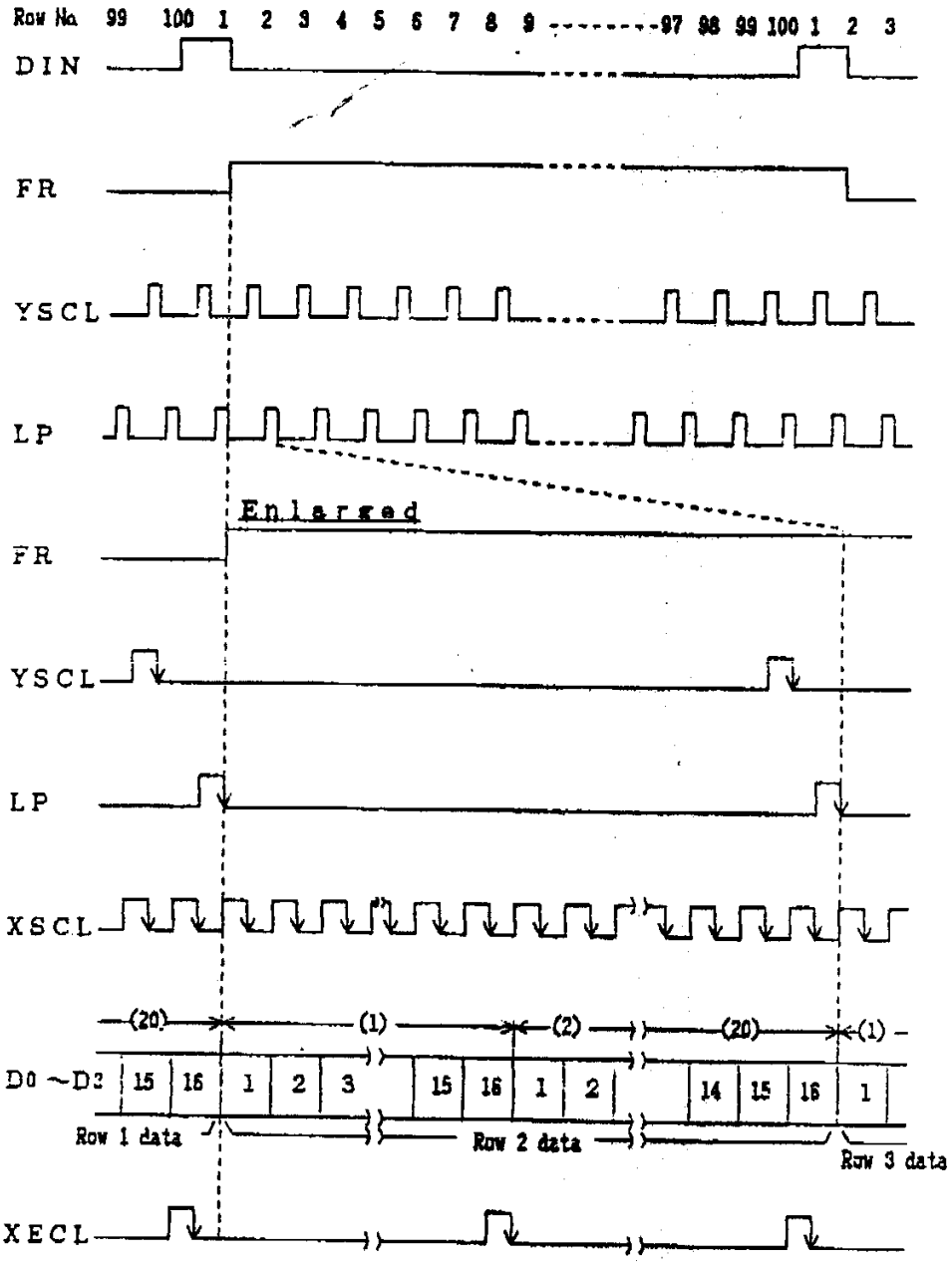
7.2.3 Relation of Input data/Output latch data



[Note] " 1, 2, - - -, 99, 100 "indicate row numbers.

16/

7.2.4 Timing Chart of Input Signals



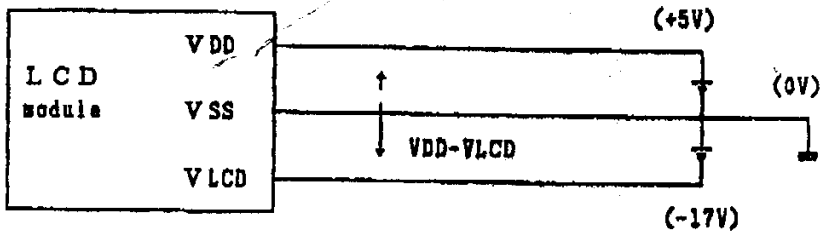
[Note 1] "(1) to (N)" of D0-D3 indicate driver chip numbers. (N=20)

[Note 2] Inthe display, D0 to D3 are located from right to left.

17

8. POWER SUPPLY AND CONTRAST ADJUSTMENT

(1) Power Supply



VDD-VLCD= LCD driving voltage

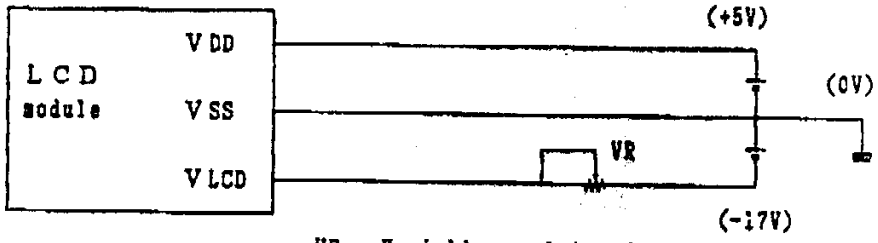
Display contrast of an LCD module depends on the voltage applied between the VDD and VLCD. Optimum display contrast can be obtained by adjusting the VLCD voltage to set a proper LCD driving voltage (VDD-VLCD).

The LCD driving voltage must be adjusted to accommodate for changes in viewing angle, ambient temterature and/or supply voltage which affect display contrast.

The effective range of supply voltage (VLCD) is approximately -4V to -17V.

(2) Typical Power Supply Circuitry

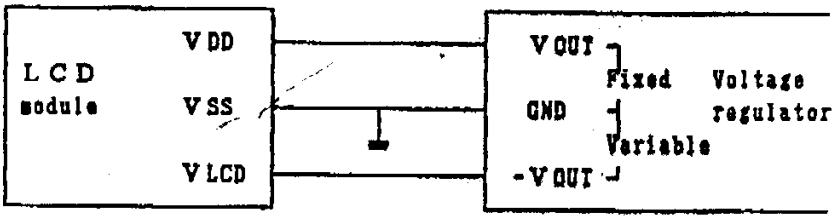
a)Non-regulated type



VR : Variable resistor for contrast adjustment

The variable resistor (VR) is used to adjust display contrast. The current flowing in the module depends on the contents of display; a current variation will cause some level of change in VLCD voltage and display contrast.

b)Regulated type



DC regulated voltages :
VOUT-GND=5V
VOUT-(-VOUT)=9V ~22V

Power is supplied by the voltage regulator. With this method, display contrast stays stable even if the contents of display change.

Display contrast can be adjusted by changing the -VOUT voltage of the voltage regulator.

19/

9. OPTICAL CHARACTERISTICS

9.1 LCD Driving Conditions

(Ta=25°C)

Voltage	Duty	Bias
15.3 V	1/100	1/9

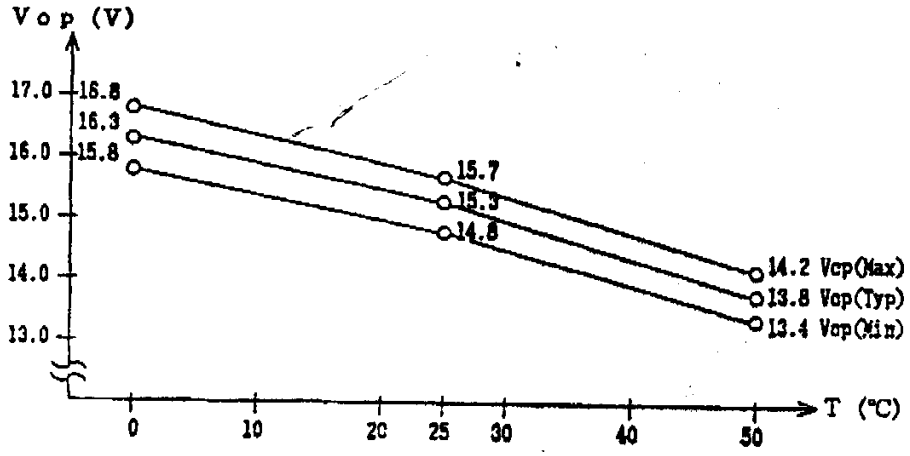
9.2 Electro-optical Characteristics

No	Prameter	Symbol	Temperature (°C)	Standard Min	Standard Typ	Standard Max	Unit	Remarks Note 1
1	Driving voltage VDD-VLCD	Vop	0	15.8	16.3	16.8	V	Note 4
			25	14.8	15.3	15.7		
			50	13.4	13.8	14.2		
2	Response time	tr	0	-	350	500	ms	Note 2
			25	-	120	180		
		tf	0	-	950	1100		
			25	-	300	400		
3	Frame frequency	fF			70		Hz	
4		θY1	25	35	-	-	Degree	Note 3
		θY2		20	-	-		
		θX1		30	-	-		
		θX2		30	-	-		
5	Contrast	K	25	6.5	7.5	-		Note 4

Note Frame frequency is defined as follows:
Common side supply voltage
peak-to-peak/2 = 1 period

20

** < Vop vs. Temperature Curves >

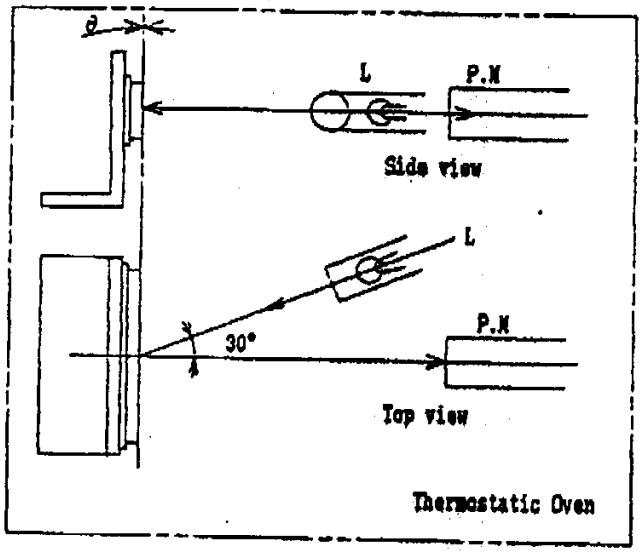


[Note 1] Optical Measuring Equipment

Equipment : Canon LC-3S brightness meter
Halogen lamp used as light source
Conditions : Spot for brightness measurement 2 mm
Spot from light source 10 mm
Angle ; θ 0°

L : Light source
P.M: Light receiver of brightness meter

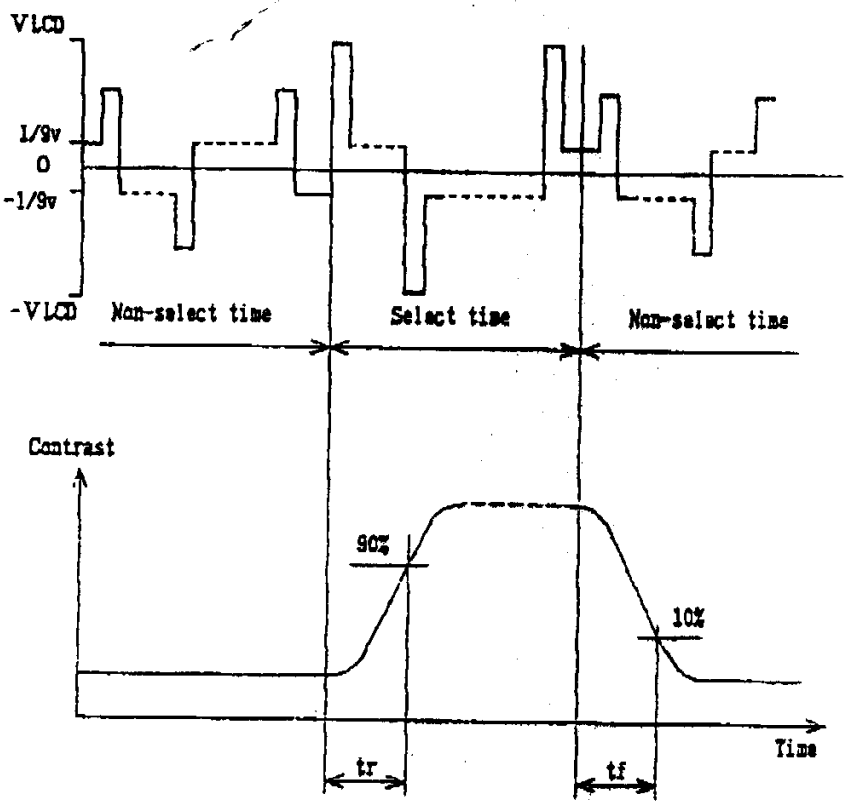
Fig. 1



21

[Note 2] Definition of response time and measuring conditions

Fig. 2



Parameter	Conditions
Ambient temperature	0 °C , 25 °C
Driving voltage	16.3 V , 15.3 V
Viewing angle	0 °
Frame frequency	70 Hz

22

[Note 3] Definition of viewing angle

Fig. 3-1

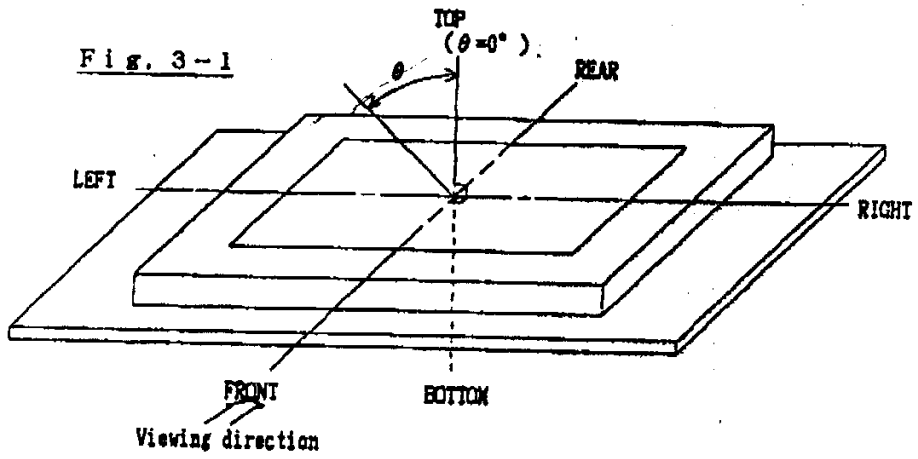
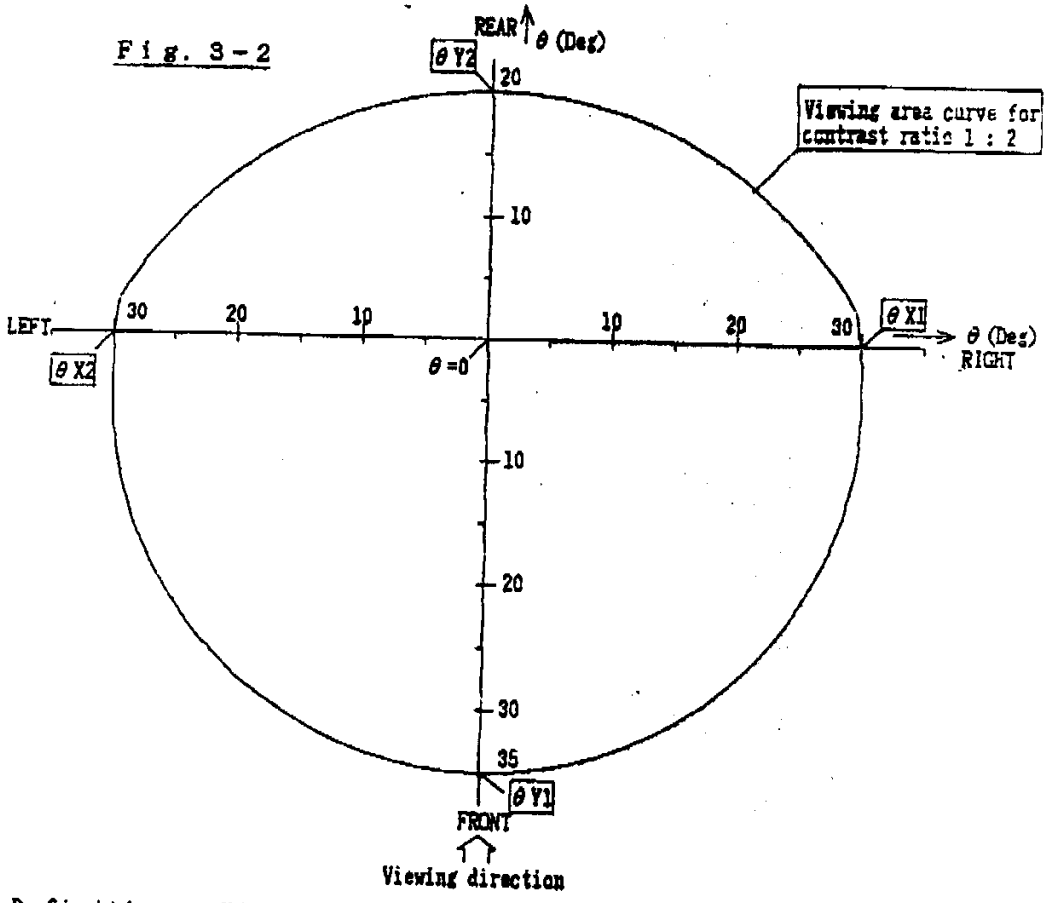


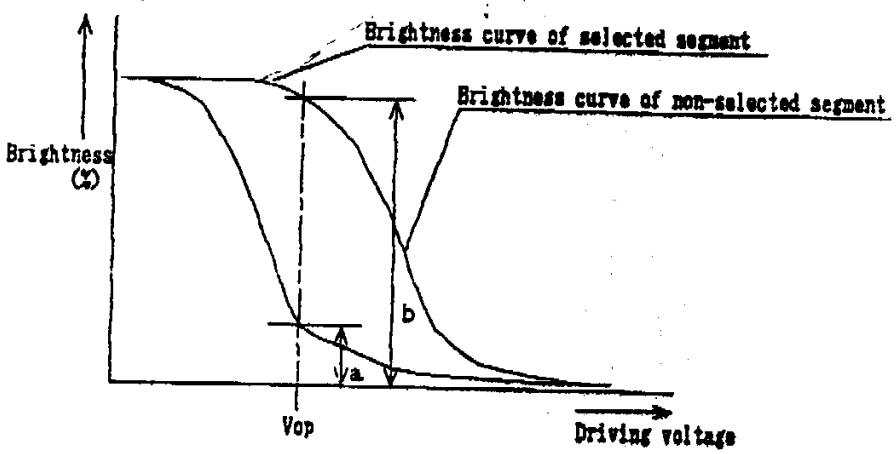
Fig. 3-2



Definition : Viewing area which gets contrast ratio 1 : 2, when operated by Vop (Typical) at 25°C .

[Note 4] Definition of contrast ratio

Fig. 4



Definition :

Contrast ratio = (Brightness in OFF state) / (Brightness in ON state) = b/a

Parameter	Conditions
Ambient temperature	25 °C
Driving voltage	15.3 V
Viewing angle	0 °

10. HANDLING PRECAUTIONS

(1) The LCD panel of EPSON LCD modules consists of two thin glass pltets with polarizers (with UV cut filters) which easily get damaged. Extreme care should be used when handling the display panel.

(2) When cleaning the display surface, use soft cloth (e.g., gauze) with a solvent (recommended below) and wipe lightly.

- isopropyl alcohol
- ethyl alcohol
- trichlorotriflorcethane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvents:
- water
- ketone
- aromatics

(3) The LCD modules use CMOS LSI drivers, so we recommend that you:

a) connect any unused input terminal to VDD or VSS;
b) do not input any signals before power is turned on; and
c) ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

(4) Modules employ LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

(5) To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

25

11. OPERATIONAL PRECAUTIONS

(1) If the LCD panel is driven on DC, the electrochemical reaction within it causes a rapid reduction in display performance. The duty 50%±1% of the FR signal must always be observed.

(2) Follow the power on/off sequence shown in Fig. 1 to prevent a latch-up or DC operation of the LCD module.

(3) No LCD module must exceed the absolute maximum ratings. If a module is operated with any value exceeding absolute maximum ratings, its performance will deteriorate and may no longer restore to normal.
In designing a system using LCD modules, utmost care should be taken of ambient temperature, input voltage signal fluctuations, supply voltage fluctuations, etc.

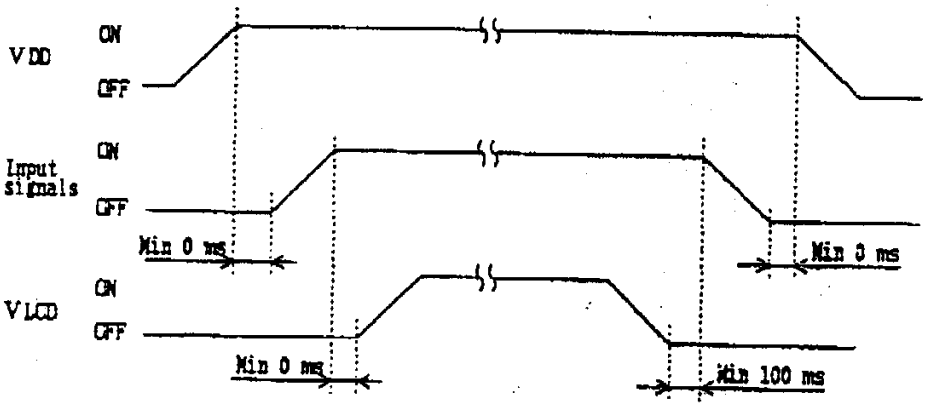


Fig. 1 Power On/Off Sequence

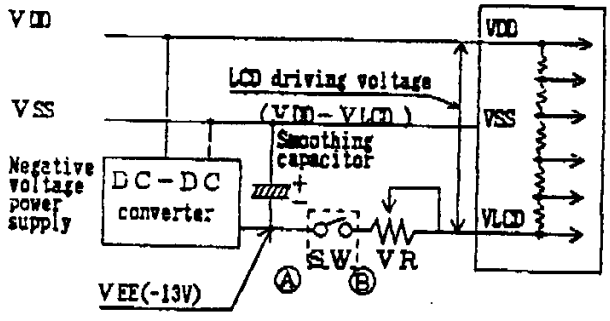


Fig. 2 Typical Power Supply Connection

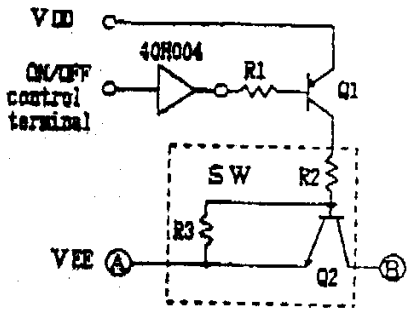


Fig. 3 Typical SW Circuit

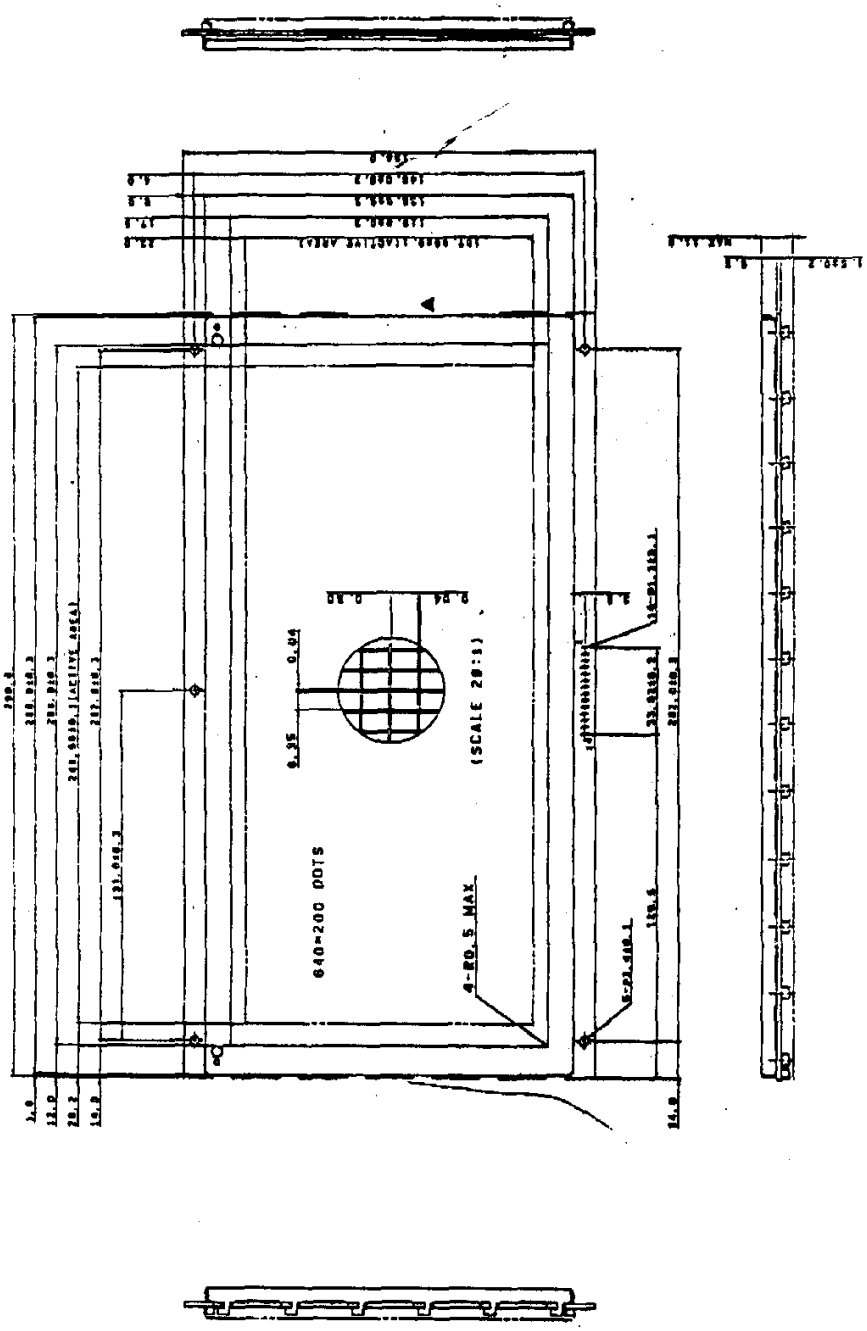
26/

[Note 1] The VLCD on/off operation shown in Fig. 1 indicates the swiching operation of Fig. 2.

[Note 2] Turning off the SW (Fig. 2) will open the VLCD terminal. Therefore, the LCD driveng voltage (VDD-VLCD) will become zero 100ms(Max.) later.

[Note 3] A typical circuit for the SW portion of Fig. 2 is given in Fig. 3 for reference.

27/27



** TOTAL PAGE.27 **